REMARKS/ARGUMENTS

Claims 1-4 are pending in the application. Reexamination and reconsideration are hereby requested.

Claims 1-2 were rejected as anticipated by Brooks. The Examiner pointed to column 6, lines 30-35 and column 7, lines 30-32 as showing a framework on the DSP.

Applicants reply that the plug-in objects of Brooks apparently create instances of algorithms (via algorithm objects) on DSPs which directly connect to the application on the host (see column 8, lines 29-32); but this does not suggest a framework on a DSP as required by claim 1.
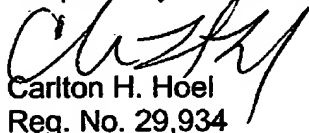
Claim 3 was rejected as unpatentable over Brooks in view of Wong.

Applicants rely on the patentability of parent claim 1.

Claim 4 was rejected as unpatentable over Fenton in view of Wong. The Examiner pointed to Fenton column 9, lines 28-33 for the designation of a second buffer by the signal processing application.

Applicants reply that Fenton is just assigning data streams to processors, not the next-frame buffer designation from the signal processing as in claim 4.

Respectfully submitted,

Carlton H. Hoel
Reg. No. 29,934
Texas Instruments Incorporated
PO Box 655474, M/S 3999
Dallas, Texas 75265
972.917.4365